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ABSTRACT

GaN electronics have hinged on invasive isolation such as mesa etching and ion implantation to define device geometry, which, however, suffer from damages, hence potential leakage paths. In this study, we propose a new paradigm of polarization isolation utilizing intrinsic electronic properties, realizing *in situ* isolation during device epitaxy without the need of post-growth processing. Specifically, adjacent III- and N-polar AlGaN/GaN heterojunctions were grown simultaneously on the patterned AlN nucleation layer on *c*-plane sapphire substrates. The two-dimensional electron gas (2DEG) was formed at III-polar regions but completely depleted in N-polar regions, thereby isolating the 2DEG channels with a large 3.5 eV barrier. Structures of polarization-isolated high electron mobility transistors (PI-HEMTs) exhibit significantly reduced isolation leakage currents by up to nearly two orders of magnitude at 50 V voltage bias compared to the state-of-the-art results. Aside from that, a high isolation breakdown voltage of 2628 V is demonstrated for the PI-HEMT structure with 3 μm isolation spacing, which is two-times higher than a conventional mesa-isolation HEMT. Moreover, the PI-HEMT device shows a low off-state leakage current of 2×10^{-8} mA/mm with a high I_{on}/I_{off} ratio of 10^9 and a nearly ideal subthreshold slope of 61 mV/dec. This work demonstrates that polarization isolation is a promising alternative toward the plasma-damage-free isolation for GaN electronics.

GaN electronics have emerged as a crucial technology for energy and communication industries due to their high breakdown voltage, fast switching speed, and high temperature (HT) operation capability.[1–6] While the geometrical size of the device shrinks, thus resulting in higher integration density, the off-state leakage current has become increasingly crucial for both discrete high electron mobility transistors (HEMTs) and a monolithic microwave integrated circuit (MMIC).[7] The damage caused by a traditional invasive device isolation process, such as mesa etching and ion implantation, is a critical leakage path.[8] Lu *et al.* proposed that in some cases, the off-state leakage current is likely to be dominated by the surface leakage current through the electrode pad on the etched GaN buffer.[9] Xu *et al.* demonstrated that there is a strong correlation between the off-state leakage current and isolation leakage current with the former being greatly suppressed via appropriate post-growth passivation.[10] Moereke *et al.* and Sun *et al.* illustrated that reduction in the leakage current in the isolation structure helps it to increase the breakdown voltage at high electric fields for the GaN HEMTs.[11,12] Herein, device isolation is an important factor in determining the device performance but is usually neglected, unfortunately.

Both mesa etching and ion implantation techniques during device fabrication suffer considerable drawbacks.[13] Mesa etching could introduce surface defects, resulting in serious surface leakage in the isolation region.[14,15] In addition, the exposed sidewall is in contact with gate electrodes, providing additional gate leakage paths for a two-dimensional-electron gas (2DEG).[16,17] The ion implantation provides an alternative option without etching, but it requires high temperature annealing to repair large lattice distortion and defects from ion bombardment.[18,19] Aside from that, implantation of light ions, such as H^+ and He^+, could cause poor thermal stability, while that of heavy ions could introduce deep level defects and cause current collapse.[20,21] Extensive efforts were devoted to reduce these defects, including dielectric passivation,[22,23] surface treatment,[24,25] and post-gate annealing.[9] However, these damages still cannot be fully removed.

Therefore, a new isolation paradigm eliminating the issues of damage or defects and enabling flexible in-plane device design in the meantime is a prospective for the development of the GaN electronics.

In this work, we demonstrated a new paradigm of polarization isolation by leveraging the 2DEG modulation capability of the opposite GaN polarity regions. The polarization isolation can be executed *in situ* epitaxially and obliterates the issues above since it does not need post-growth etching and ion implantation. The band structure and isolation characteristics of the polarization isolation scheme were investigated both theoretically and experimentally.

Depending on the lattice orientation, the polar III-nitride devices are either metal (III)- or nitrogen (N)-polarity. Currently, most electronic and optical devices have been made with either polarity, including the GaN HEMTs.[26–29] It is important to note that the 2DEG distribution in the III- and N-polar GaN HEMTs is determined by the direction of spontaneous polarization and, consequently, the band bending at the AlGaN/GaN interface.[1,30–32] If III-polar and N-polar domains are oriented side-by-side in one wafer, the 2DEG at the AlGaN/GaN heterojunction can be selectively induced or depleted. The unique structure combining both III- and N-polar regions is herein referred to as the "lateral polarity structure (LPS)."[33,34] This architecture can take full advantage of different polarity domains, providing novel perspectives in the design and fabrication of optoelectronic and electronic devices such as super-junctions,[35] Schottky barrier diodes (SBDs),[36] MESFETs,[37] and photodetectors.[38] In this work, specifically, the incorporation of the LPS into the HEMT device can act as an efficient isolation region in the absence of plasma-related damages, thus greatly benefiting device performance.

The epitaxial structures were grown on 2-in. c-plane sapphire substrates by a metal organic chemical vapor deposition (MOCVD) system. Trimethylaluminum, trimethylgallium, and ammonia were used as the Al, Ga, and N sources, respectively. A conventional III-polar HEMT was grown on the substrate with a uniform 20 nm AlN nucleation layer (NL), while our proposed polarization-isolated (PI)-HEMT was grown on the substrate with a patterned AlN NL. Special care was taken before epitaxial growth, in which case substrates with a uniform or patterned AlN NL were treated with H_2 annealing for 2 min at 1000 °C and NH_3 nitridation for 5 min at the same temperature. The epitaxial structure consists of a 30 nm $Al_{0.3}Ga_{0.7}N$ barrier layer, a 2 nm AlN insertion layer, a 100 nm GaN channel layer, a 1.5 μm high temperature (HT) AlN buffer layer, and a patterned AlN NL from top to the bottom, as shown in Fig. 1(a). III-polar and N-polar domains were grown on the NL and bare sapphire, respectively. The Ti/Al/Ni/Au source and drain contacts were then deposited by e-beam evaporation followed by rapid thermal annealing at 800 °C for 60 s in N_2 ambient. After that, a Ni/Au gate electrode was deposited. The gate length (L_G) is fixed at 3 μm. The gate-to-source distance (L_{GS}) is 2 μm, and the gate-to-drain distance (L_{GD}) is 3 μm.

A uniform III-polar AlGaN/GaN HEMT with exactly the same structure was also prepared. The 2DEG sheet carrier concentration

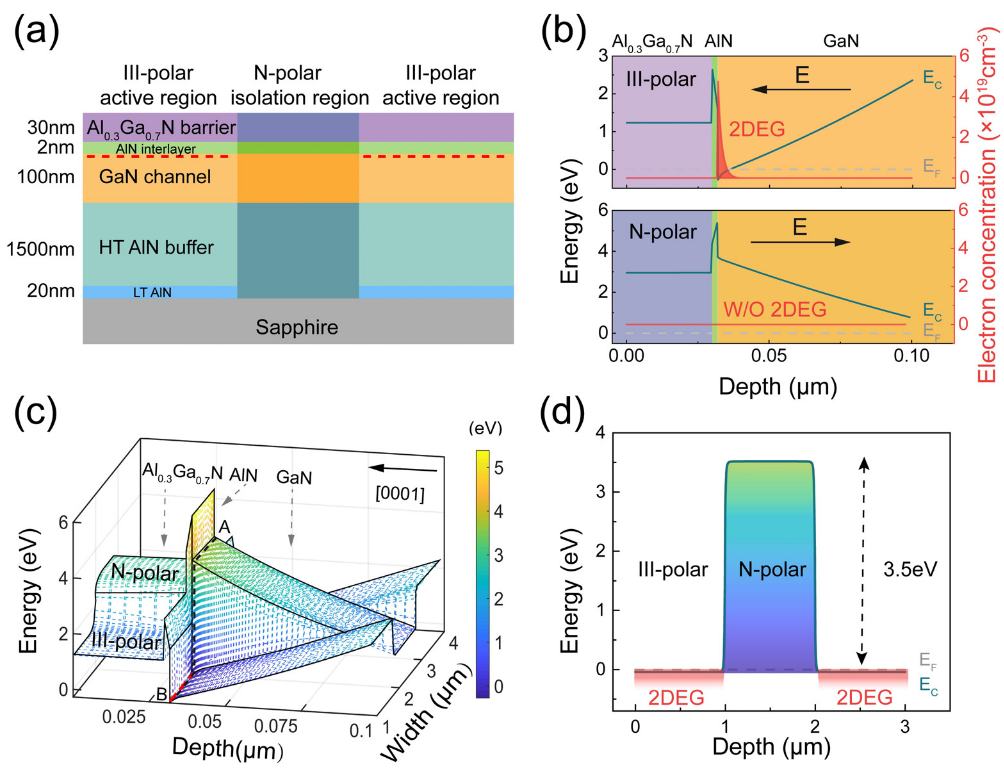

FIG. 1. (a) The cross-sectional schematic structure of the PI-HEMT structure with in-plane distributed III and N-polar domains. The red dashed line represents the 2DEG. (b) Band diagrams of the III- and N-polar regions. (c) The 3D mapping of the conduction band showing the barrier height between III- and N-polar GaN of the PI-HEMT structure with the N-polar width (i.e., isolation spacing) of 1 μm. (d) Conduction band diagram extracted from the dashed line A–B in (c).

and carrier mobility are $-1.5 \times 10^{13}/\text{cm}^2$ and $1277\ \text{cm}^2/\text{V}\cdot\text{s}$, respectively, and the sheet resistance is 326 Ω/sq. Due to the large lattice mismatch between the GaN channel and AlN buffer, the quality of the GaN channel layer is deteriorated, leading to scattering effects and reduced carrier mobility.[39,40] Supplementary material Fig. S1 illustrates the rocking curves (RCs) for the GaN channel layer and reciprocal space mapping of the whole structure.

Figure 1(b) illustrates the conduction band diagram of III-polar and N-polar HEMT structures with and without 2DEG formation in the AlGaN/GaN interface, respectively. The conduction band of the GaN channel layer of the PI-HEMT structure is below the Fermi level inducing the 2DEG, while for the N-polar counterpart, the conduction band is above the Fermi level with depletion of the 2DEG. Due to inversion of the spontaneous polarization direction, the polarization-induced electric field in the III-polar structure is opposite to that of the N-polar structure. More details about the conduction band diagrams can be found in supplementary material Fig. S2. Moreover, the 2D band diagram in Fig. 1(b) could be further plotted into a three-dimensional (3D) band diagram in Fig. 1(c), showing the combination of the vertical heterojunction and lateral homojunction. It is apparent that the elevated band of the N-polar region adjacent to the 2DEG of the III-polar region provides large barrier height, strictly limiting the lateral flow of the 2DEG to the N-polar region. Figure 1(d) shows that the barrier height is approximately 3.5 eV, significantly larger than the conduction band offset between AlN and GaN. From the point of view of the charge distribution, a high concentration of the 2DEG is induced by the fixed positive charge in the barrier layer at the interface of the III-polar heterojunction. Due to the inversed direction of spontaneous polarization, a negative polarization charge at the bottom of the barrier layer leads to electron depletion and an elevated conduction band of the GaN channel layer in the N-polar domain, responsible for the high lateral barrier height. The distributions of electrons in uniform III-polar and PI-HEMTs are shown in supplementary material Fig. S3.

Cross-sectional transmission electron microscopy (TEM) images are shown in Figs. 2(a) and 2(b). The thicknesses of different epitaxial layers are within expectation. Figure 2(c) shows the high-resolution TEM image at the boundaries between III- and N-polar domains, where opposite orientations of the atoms were unambiguously confirmed. The [0001] direction is defined along the III-polarity, whereas the [000–1] direction is along the N-polarity. A sharp and straight inversion domain boundary (IDB) is observed in the HRTEM image, stemming from the boundary of the patterned AlN nucleation layer. A smooth transition between the III-polar and N-polar regions occurs at the length scale of only a few nanometers. Ordered atomic arrangement is a strong indication of the high-quality IDB interface in the absence of destructive dislocations. Our findings are consistent with the reports from Liu *et al.* and Pezzagna *et al.*, in which case a high-quality IDB interface was obtained on a *c*-sapphire substrate by MOCVD.[41,42] Furthermore, wet etch has been typically used for verification of surface polarity in III-nitride thin films.[42,43] The N-polar surface is susceptible to an aqueous solution of KOH, while the III-polar surface remains inert to etchant due to opposite atom orientations in III- and N-polar domains. Thus, 3 mol/L KOH etching in 80 °C for 10 min was applied to verify the polarity of PI-HEMTs as a complement to TEM analysis. The height difference between the device region and isolation region before and after KOH etching was compared. As shown in supplementary material Fig. S4, the height

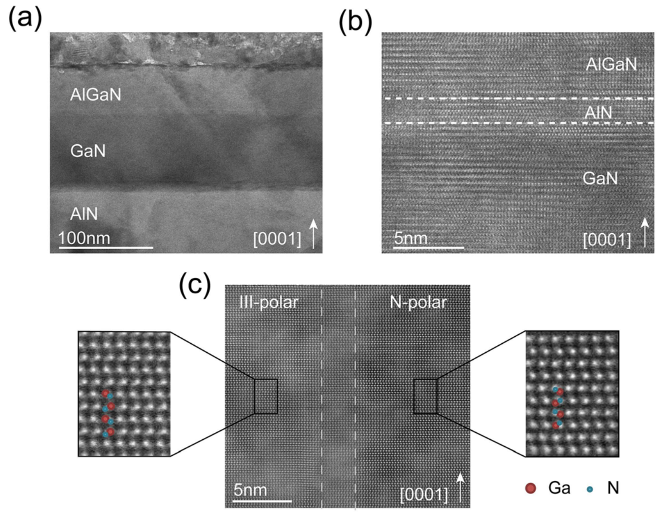

FIG. 2. (a) Cross-sectional high-resolution TEM image and (b) atomic-resolution image of the III-polar active region. (c) Lateral distributed III- and N-polar domains in the high-resolution TEM image, where metal and nitrogen atoms are denoted by the red and blue circles.

difference at the domain boundary was increased to approximately 700 nm after KOH etching, confirming the N-polarity nature of the isolation region.

The isolation leakage current (I_{iso}) can represent the performance of a given isolation technique and herein deserves in-depth investigations. PI-HEMT samples were grown where two III-polar active regions were separated by one N-polar isolation region with its isolation spacing (W_d) of 3, 10, and 100 μm. The isolation leakage (I_{iso}) vs applied bias (V) between the two active regions is shown in Fig. 3(a). When $W_d = 100\ \mu$m, I_{iso} remains as low as 10^{-13} A/mm. As W_d decreases to 10 and 3 μm, respectively, I_{iso} increases with bias and becomes saturated at 2×10^{-12} and 2×10^{-10} A/mm beyond 40 V. For comparison, two uniform III-polar HEMTs with the same structure were grown, and mesas were obtained by plasma etching with a depth of 120 nm. Isolation spacing W_d of the two samples are 3, 10, and 100 μm. Afterwards, HCl passivation was applied to one of the mesa-isolated samples. The isolation leakages were then measured at two-terminal bias of 100 V shown in Fig. 3(b). Clearly, I_{iso} are comparable among all three samples at an isolation spacing of 100 μm, suggesting that both mesa etching and polarization isolation are suitable for larger-scale device isolation. However, when the isolation spacing is reduced to 3 and 10 μm, the average I_{iso} of the PI-HEMT structures are 1.7×10^{-10} and 3.8×10^{-12} A/mm, significantly smaller than those of the etched mesas. The reason is that surface defects caused by plasma etching introduce a major leakage path. With smaller W_d, the leakage becomes increasingly dominated by the surface defects. Figure 3(c) clearly illustrated that I_{iso} is linearly dependent on W_d. Figure 3(d) compares the state-of-the-art isolation leakage currents with various W_d.[9,10,25,44–47] At the spacing of 10 μm, the proposed polarization isolation technique outperforms other reports by one or two orders of magnitude especially at 10 and 50 V. At 100 V, the result with 10 μm polarization isolation is on par with the lowest reported leakage current, which is associated with four-times larger W_d.

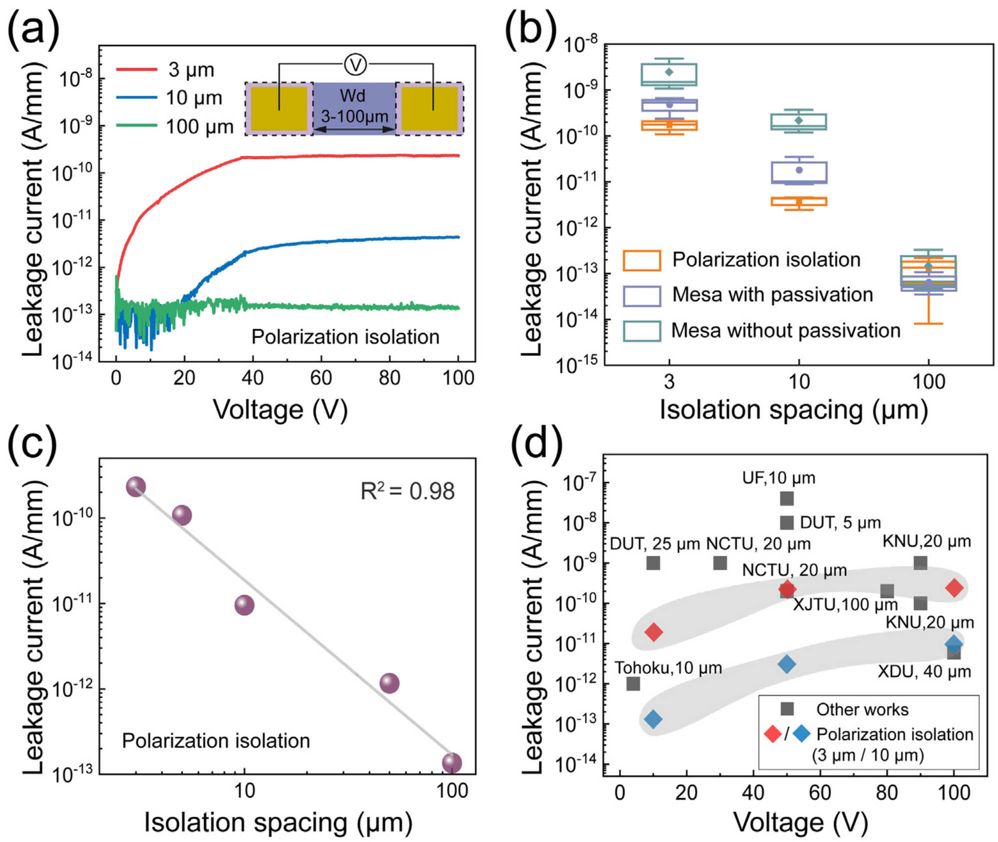

FIG. 3. (a) I_{iso}–V characteristics of the PI-HEMT structures with the W_d of 3, 10, and 100 μm. (b) I_{iso} comparison of the PI-HEMT structures and the mesa-isolated III-polar HEMT structures with the W_d of 3, 10, and 100 μm; (c) dependence of I_{iso} on W_d of the PI-HEMT structures with a W_d of 3–100 μm at V = 100 V. (d) Benchmarking of I_{iso} vs state-of-the-art results with different W_d.

The comparison of I_{iso} distinctly demonstrates the advantage of the polarization isolation for GaN electronics.

Note that the two-terminal breakdown voltage is also a critical factor in determining the isolation characteristic of the device. Furthermore, the increase in the isolation breakdown voltage helps us to improve the three-terminal breakdown property of the device.[12] For the PI-HEMT structures and the mesa-isolated III-polar HEMT structures, the two-terminal breakdown characteristics were measured and compared with a W_d of only 3 μm exemplarily shown in Fig. 4. The breakdown voltages (V_{BR}) of the mesa-isolated HEMT structures without and with HCl passivation are 1380 and 1644 V, respectively. For the PI-HEMT structure with $W_d = 3\ \mu$m, a much larger breakdown voltage of 2628 V is revealed thanks to the absence of the surface defects induced by plasma etching. Table I summarizes the breakdown voltages with the W_d of 3, 10, and 100 μm. With a W_d of 10 μm, the V_{BR} of the mesa-isolated III-polar HEMT structures are both below 3000 V, while no breakdown was observed for the PI-HEMT structures. With a W_d of 100 μm, none of the samples broke down. The results suggest that the polarization isolation is highly advantageous in high-density high-power device integration.

Top-view scanning electron microscope (SEM) images of a PI-HEMT device prior to and after the electrode deposition are shown in Figs. 5(a) and 5(b), respectively. The output and transfer characteristics of the PI-HEMT device were further shown in Figs. 5(c) and 5(d). The threshold voltage is estimated to be −6.9 V using linear extrapolation of the transfer curve. The more negative threshold voltage is mainly due to the thicker AlGaN barrier layer, which required larger gate bias to deplete the 2DEG. The off-state leakage current (I_{off}) is $\sim 2 \times 10^{-8}$ mA/mm with the I_{on}/I_{off} ratio of 10^9. It is noted that the I_{off} is almost equal to the gate leakage current, indicating that the I_{off} is dominated by the gate leakage, while the other leakages are negligible. The subthreshold slope $\{SS = dV_G/d[\log(I_D)]\}$ obtained from Fig. 5(d) is 61 mV per decade, very close to the theoretical limit of 60 mV/dec.[48] Finally, the PI-HEMT reported in this work is only a prototype architecture without gate dielectrics or field plates but still surprisingly shows a low off-state leakage current of 2×10^{-8} mA/mm. The result unambiguously demonstrates the excellent leakage suppression of the PI-HEMT device, revealing the unique advantage of utilizing polarization modulation to tune the 2DEG in-plane.

In conclusion, a new paradigm of the device isolation by polarization was proposed for GaN electronics by taking advantage of the opposite polarization directions in the III- and N-polar regions. The isolation current of the PI-HEMT structures is two orders of magnitude lower than mesa isolation thanks to the absence of plasma-related damages.

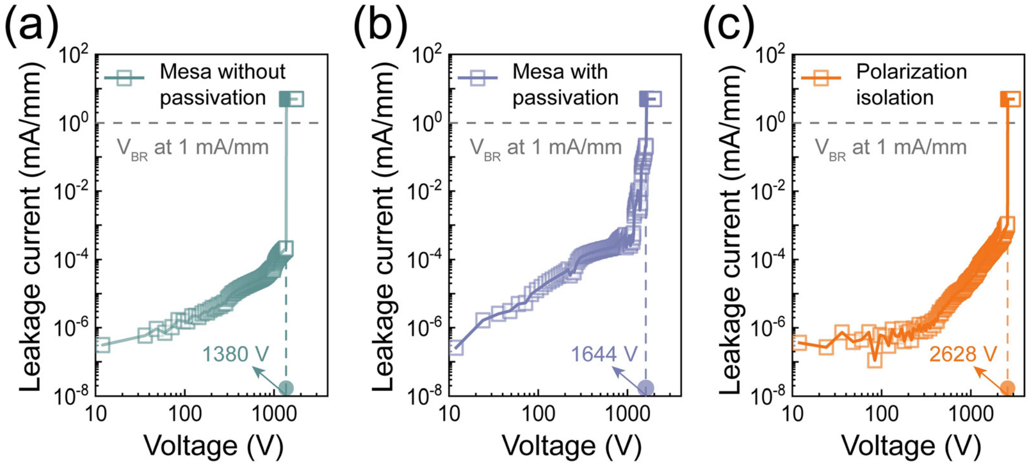

FIG. 4. Two-terminal breakdown characteristics with a W_d of 3 μm. I–V characteristics of the mesa-isolated HEMT structures without (a) and with (b) HCl passivation as well as the PI-HEMT structure (c).

TABLE I. Breakdown voltages (V_{BR}) of the polarization isolation and mesa etching samples at different isolation spacings extracted at a leakage current of 1 mA/mm.[a]

	3 μm	10 μm	100 μm
Mesa without passivation	1380 V	1920 V	NA
Mesa with passivation	1644 V	2580 V	NA
Polarization isolation	2628 V	NA	NA

[a]"NA" represents no breakdown at 3000 V, the upper limit of the equipment.

A high breakdown voltage of 2628 V was demonstrated for the PI-HEMT structure at the isolation spacing of 3 μm, which is two-times higher than the conventional mesa-isolation HEMT. The PI-HEMT device exhibits a low off-state leakage current of 2×10^{-8} mA/mm, a high I_{on}/I_{off} of 10^9, and a nearly ideal subthreshold slope of 61 mV/dec. These results clearly demonstrate that the polarization isolation is extremely promising in the development of GaN power electronic arrays toward high breakdown voltage and high-density chip integration.

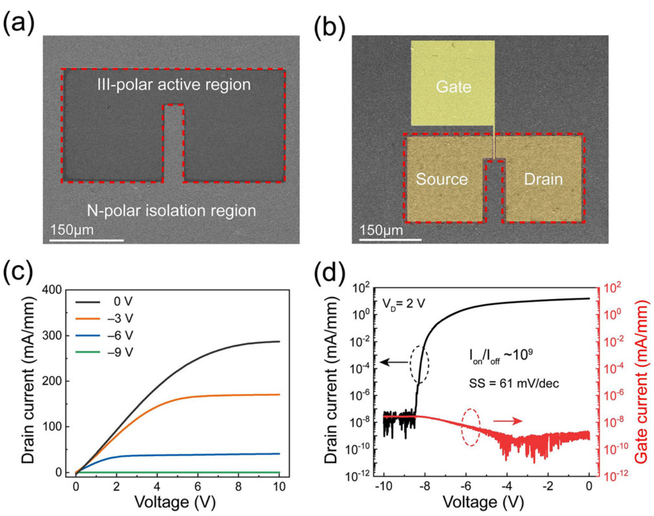

FIG. 5. Top-view SEM images prior to (a) and after (b) electrode deposition. (c) Output characteristics with gate voltage changed from −9 to 0 V with a step of −3 V. (d) Transfer characteristic and gate leakage current.

See the supplementary material for detailed rocking curves (RCs) for the GaN channel layer, the reciprocal space mapping for amid partial relaxation between GaN and AlN, the conduction band diagrams for different polar heterojunctions, and the distribution of 2DEG for uniform III-polar and PI-HEMT.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Yijun Dai: Data curation (lead); Investigation (lead); Writing – original draft (lead). **Xiaohang Li:** Investigation (equal); Writing – review and editing (equal). **Jichun Ye:** Supervision (equal); Writing – review and editing (equal). **Wei Guo:** Funding acquisition (lead); Investigation (lead); Project administration (lead); Writing – review and editing (lead). **Li Chen:** Data curation (equal); Formal analysis (equal). **Houqiang Xu:** Data curation (equal); Formal analysis (equal); Investigation (equal). **Feras AlQatari:** Formal analysis (equal); Investigation (equal). **Chenyu Guo:** Formal analysis (equal); Investigation (equal). **Xianchun Peng:** Data curation (equal); Investigation (equal). **Ke Tang:** Investigation (equal); Methodology (equal). **Che-Hao Liao:** Investigation (equal); Methodology (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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