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ABSTRACT

In this Letter, we report on a monolithically integrated β-Ga_2O_3 NMOS inverter integrated circuit (IC) based on heteroepitaxial enhancement mode (E-mode) β-Ga_2O_3 metal-oxide-semiconductor field-effect transistors on low-cost sapphire substrates. A gate recess technique was employed to deplete the channel for E-mode operation. The E-mode devices showed an on-off ratio of $\sim 10^5$ with a threshold voltage of 3 V. In comparison, control devices without the gate recess exhibited a depletion mode (D-mode) with a threshold voltage of −3.8 V. Furthermore, depletion-load NMOS inverter ICs were fabricated by monolithically integrating D- and E-mode transistors on the same substrate. These NMOS ICs demonstrated inverter logic operation with a voltage gain of 2.5 at $V_{DD} = 9$ V, comparable with recent GaN and other wide-bandgap semiconductor-based inverters. This work lays the foundation for heteroepitaxial low-cost and scalable β-Ga_2O_3 ICs for monolithic integration with (ultra)wide bandgap Ga_2O_3 power devices.

β-Ga_2O_3 is a promising material for low-loss power switching and radio frequency power amplification due to its high critical electric field of ∼8 MV/cm and large Baliga/Johnson figures of merit.[1–5] Moreover, β-Ga_2O_3 can accommodate a wide range of n-type doping concentrations from semi-insulating ($\sim 10^{15}$–10^{16} cm^{-3}) to highly doped ($\sim 10^{18}$–10^{20} cm^{-3}).[6,7] In the past decade, β-Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) have been widely investigated, and significant progress in key device characteristics has been made.[3,4,8] However, commercial applications in low-loss power converters operating at high frequency and harsh environments require efficient and miniaturized β-Ga_2O_3 power electronics.[9] However, the current power electronics are based on (ultra)wide bandgap (UWBG) semiconductor-based power devices, externally connected to Si-based logic. This results in high inductance parasitic losses and large module sizes, which limit the overall performance of the power module.[10] Moreover, a Si-based controller limits its applications in harsh environments. Therefore, the development of a UWBG β-Ga_2O_3 logic driver is essential for monolithic integration with a Ga_2O_3 power device to obtain miniaturized and efficient β-Ga_2O_3 power electronics.[9]

On the other hand, the current studies on β-Ga_2O_3 devices are based on homoepitaxial Ga_2O_3 thin films grown on native substrates, which yield excellent material quality but possess relatively high cost and small substrate size, which impedes their future scalability. On the contrary, heteroepitaxial devices on more commercially viable substrates, such as sapphire and silicon, could largely address these issues.[11–14] Those substrates have proven to be instrumental in the commercial success of wide bandgap compound semiconductor devices. For instance, most commercial GaN-based light-emitting diodes and high-electron-mobility transistors (HEMTs) are heteroepitaxially grown on sapphire and silicon substrates, whereas similarly the bulk GaN substrates offer superior material quality but suffer from high cost and low scalability.[15,16] Therefore, the heteroepitaxial UWBG β-Ga_2O_3 logic driver is essential to realize miniaturized, scalable, and efficient β-Ga_2O_3 power electronics. However, with the future availability of low-cost and large-area Ga_2O_3 substrates, efficient homoepitaxial β-Ga_2O_3 power electronics could be realized similarly.

For a logic driver, the realization of a Ga_2O_3 complementary metal oxide semiconductor (CMOS) is challenging because of the absence of p-type Ga_2O_3. However, the monolithic integration of depletion mode (D-mode) and enhancement mode (E-mode) Ga_2O_3 MOSFETs can realize an n-channel metal oxide semiconductor (NMOS) logic, also known as direct coupled FET logic (DCFL).[10]

There are several reports on heteroepitaxial Ga_2O_3 MOSFETs.[17,18] Yet, they are limited to the D-mode only. However, E-mode transistors are indispensable for practical NMOS logic applications due to their low OFF-state power dissipation. Some techniques, such as channel thinning, light channel doping, and gate recess, have been used for the E-mode operation of Ga_2O_3 transistors on native substrates.[4,19] The first two could result in a lower ON current, while the gate recess technique requires a critically smooth recess profile. To date, no study on the E-mode heteroepitaxial Ga_2O_3 MOSFETs and NMOS logic integrated circuits (ICs) has been reported.

In this study, we demonstrated the heteroepitaxial E-mode Ga_2O_3 transistors based on atomically smooth gate recess. Moreover, the Ga_2O_3 NMOS inverter ICs were fabricated using monolithic integration of D- and E-mode MOSFETs on the same sapphire substrate. This NMOS IC can be monolithically integrated with other (ultra)wide bandgap devices for future practical applications.

Figure 1(a) shows the cross-sectional schematic of recessed gate MOSFETs. Initially, Si-doped β-Ga_2O_3 was epitaxially grown on c-sapphire substrates using pulsed laser deposition at a growth temperature of 700 °C. A laser ablation frequency of 5 Hz, an oxygen partial pressure of 4 mTorr, and a laser energy of 100 mJ remained constant during growth. 3D schematics of both non-recessed and recessed MOSFETs are shown in Figs. 1(b) and 1(c), respectively. The fabrication process flow of both MOSFETs is illustrated in Fig. 1(d). The same fabrication process was applied to both devices, except an additional step to form the recess in the recessed MOSFETs. The transistors were fabricated on 50 nm thick epitaxially grown Ga_2O_3 films on sapphire substrates.

The device fabrication was started by isolating the Ga_2O_3 channel using BCl_3/Ar ICP-RIE dry etching with a photoresist mask. For recessed gate MOSFETs, a 5 μm long gate recess was defined using optical lithography, and BCl_3-based slow dry etching was used to form the recess structure. The samples were, subsequently, cleaned using piranha to remove any residual photoresist and obtain a smooth surface morphology. Then, a Ti/Au (20/100 nm) source-drain (SD) contact was formed following the standard lithography process, metal deposition, and liftoff. Next, a 25 nm Al_2O_3 gate dielectric was deposited using plasma-enhanced atomic layer deposition (PEALD) at the growth temperature of 250 °C. Then, SD contact regions were selectively opened from the Al_2O_3 dielectric using optical lithography and BCl_3-based dry etching. Finally, a Ti/Au (20/100 nm) gate metal contact was formed using the same standard process, as discussed above for SD formation. Figure 1(e) shows a scanning electron microscopy (SEM) top view of the fabricated transistor.

Figure 2(a) shows the x-ray diffraction (XRD) pattern of the β-Ga_2O_3 film on the sapphire. β-Ga_2O_3 (−201), (−402), and (−603) XRD peaks confirm the mono-orientation of the β-Ga_2O_3 film on the heterogeneous sapphire substrate. The surface morphology of the grown film was investigated using atomic force microscopy (AFM). A smooth surface with an RMS roughness of 0.8 nm can be observed in Fig. 2(b). Figure 2(c) shows the AFM profile of the recessed structure, depicting a recess depth of 11 nm (inset) with an RMS roughness of 0.6 nm (inside recess), as shown in Fig. 2(d). Achieving a smooth surface morphology is highly critical for E-mode MOSFETs, attributed to a slow dry etching of 11 nm/min. Figures 2(e) and 2(f) show scanning transmission electron microscopy (STEM) images. The sidewall and bottom facets of the gate recess interface are identically smooth,

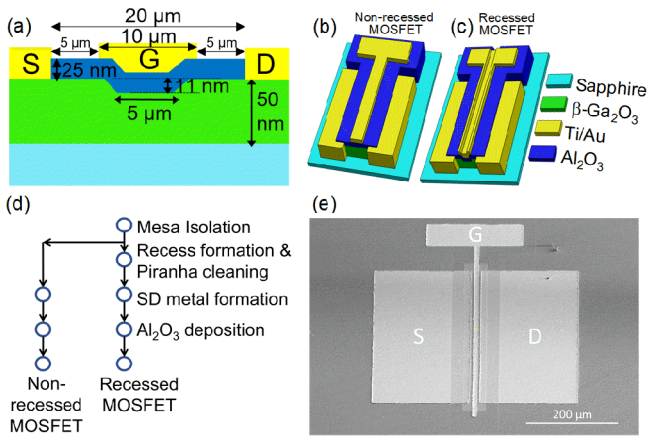

FIG. 1. Cross-sectional view of (a) the recessed gate. 3D schematics of (b) non-recessed and (c) recessed gates. (d) Fabrication process flow. (e) Scanning electron microscopy (SEM) top view of the β-Ga_2O_3 MOSFETs.

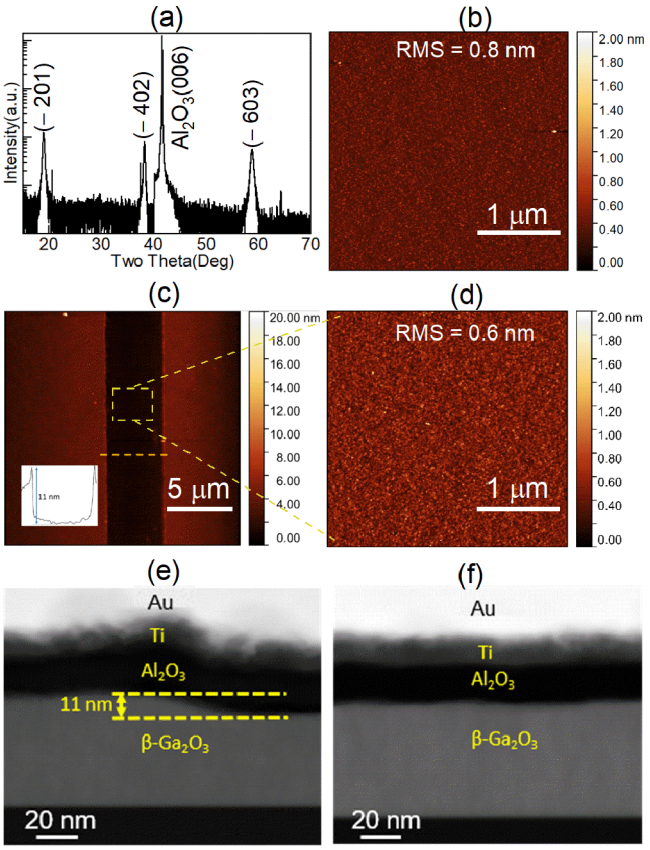

FIG. 2. β-Ga_2O_3 film characterization: (a) x-ray diffraction and (b) atomic force microscopy (AFM) image. AFM image of (c) the recess profile, (c-inset) recess depth, and(d) surface topography (inside recess). Scanning transmission electron microscopy (STEM) image of (e) the sidewall (highlighting a recess depth of 11 nm) and (f) the bottom facet of gate recess.

showing an identical recess depth of ~11 nm, which is consistent with AFM measurement. The electron concentration and mobility of the β-Ga_2O_3 film were 5×10^{18} cm^{-3} and 0.38 cm^2 V^{-1} s^{-1}, respectively, determined by Hall-effect measurements. Electrical characterization of the fabricated MOSFETs was performed using a 4200-semiconductor parameter analyzer at RT. Both recessed and non-recessed MOSFETs have identical channel length $L_{CH} = 20\ \mu$m, channel width $W_{CH} = 500\ \mu$m, and gate length $L_G = 10\ \mu$m.

Figures 3(a) and 3(c) show the logarithmic transfer behavior of non-recessed and recessed MOSFETs, respectively, at different drain-source voltages (V_{DS}). Both devices exhibit negligible gate-source current I_{GS}. The threshold voltages $V_{TH} = -3.8$ and 3 V were obtained for non-recessed and recessed MOSFETs, at $V_{DS} = 5$ V, calculated from the linear-scale transfer curve shown in Figs. 3(a) and 3(c), respectively. Both MOSFETs have a similar ON/OFF ratio of $1 \pm 0.2 \times 10^5$ and a subthreshold swing (SS) of 1.2 ± 0.2 V/decade. This high SS value can be attributed to the high density of Al_2O_3/Ga_2O_3 interface trap states. The upper limit of the interface trap state density can be estimated using the following equation:[4,20]

$$D_{it} = \left(\frac{SS \times q}{\ln(10) \times KT} - 1\right)\frac{C_{ox}}{q}, \tag{1}$$

where D_{it} is the interface state density, q is the electron charge, K is Boltzmann's constant, and C_{ox} is the oxide capacitance.

The calculated value of D_{it} is 1.6×10^{13} cm^{-2}eV^{-1}, consistent with other reported Al_2O_3/Ga_2O_3 interface studies.[17,21,22] SS and I_{GS} are similar for both the non-recessed and recessed MOSFETs, which confirms that the optimized recess etching does not worsen the Ga_2O_3 film roughness and, hence, the Al_2O_3/Ga_2O_3 interface, compared with the non-recessed case.

Figures 3(b) and 3(d) show the output characteristics of the non-recessed and recessed MOSFETs, respectively, for different gate-source voltages (V_{GS}). The maximum drain current density $(I_{DS})_{max}$ at $V_{GS} = 5$ V is four times larger in the non-recessed than recessed MOSFETs. Furthermore, the ON resistances were $R_{on} = 190$ and 405 kΩ·cm of non-recessed and recessed MOSFETs, respectively, calculated from the output curve at $V_{GS} = 5$ V. An OFF-state breakdown voltage was ~85 V in both the non-recessed and recessed MOSFETs. It was limited by the dielectric breakdown, as confirmed by the gate leakage current after performing the breakdown measurement.

Figures 4(a) and 4(b) show the hysteresis transfer behavior of the non-recessed and recessed MOSFETs, respectively, at $V_{DS} = 5$ V. A large hysteresis width of ~2 V was obtained in both cases, which again confirms the high density of the interface trap charges that can be estimated using the following equation:

$$N_{it} = \frac{|V_{Hy,T}| \times C_{ox}}{q}, \tag{2}$$

where N_{it} is the interface trap charge density and $V_{Hy,T}$ is the hysteresis voltage width at the threshold.

The calculated value of N_{it} was ~10^{13} cm^{-2} consistent with our D_{it} results and other homoepitaxial Ga_2O_3 MOSFET reports.[23]

To understand the E-mode operation in the recessed MOSFETs, the one-dimensional depletion depth was calculated using the depletion approximation.[4] The depletion depth under the gate region $(W_{it})_{gated}$ can be calculated using

$$(W_{it})_{gated} = \left[\frac{2\epsilon_0\epsilon_r V_{FB}}{qN_d}\right]^{\frac{1}{2}}, \tag{3}$$

where ϵ_0 and ϵ_r are the vacuum and relative permittivity, respectively, N_d is the electron carrier concentration, and V_{FB} is the flatband voltage.

The flatband voltage V_{FB} can be estimated using the following equation:

$$V_{FB} = \phi_{ms} + \frac{Q_{it}}{C_{ox}}. \tag{4}$$

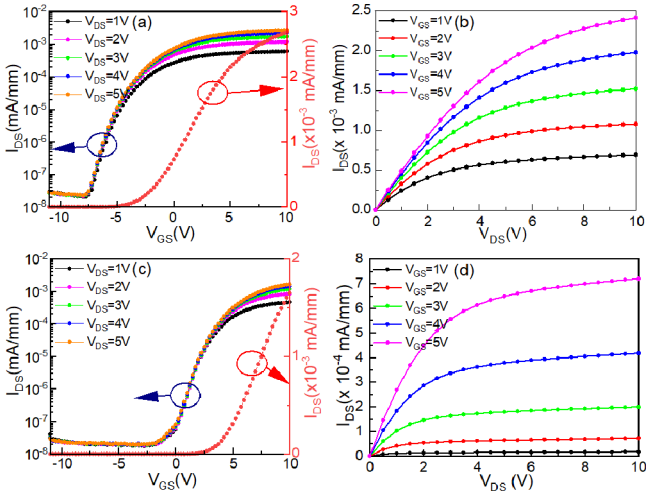

FIG. 3. Transfer (logarithmic and linear) and output characteristics, respectively, (a) and (b) non-recessed and (c) and (d) recessed MOSFETs at different drain-source (V_{DS}) and gate-source voltages (V_{GS}). Linear transfer behavior is at $V_{DS} = 5$ V, shown in (a) and (c).

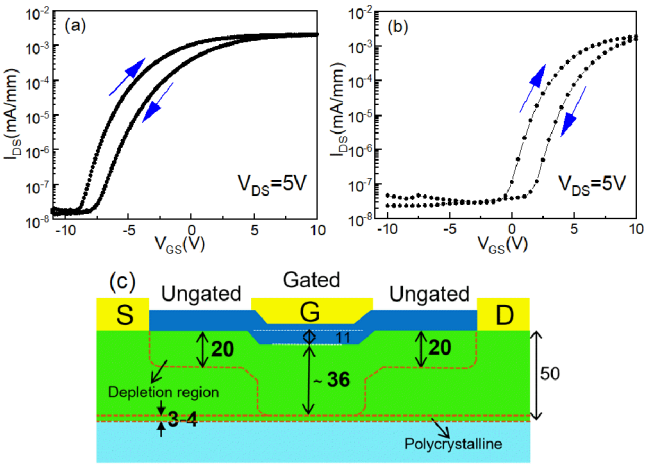

FIG. 4. Hysteresis transfer behavior of MOSFETs (in the logarithmic scale): (a) non-recessed and (b) recessed gate. (c) Cross-sectional schematic of depletion depths explaining the mechanism of E-mode operation of recessed MOSFETs. (All numbers are in nm.)

The depletion depth of the ungated region $(W_{it})_{ungated}$ can be calculated using

$$(W_{it})_{ungated} = \frac{Q_{it}}{N_D}. \quad (5)$$

$V_{FB} = 6$ V was used in the analysis. The top side depletion depth $(W_{it})_{gated}$ and $(W_{it})_{ungated}$ are ~36 and ~20 nm, were calculated using Eqs. (3) and (5), respectively. The bottom side depletion depth will be negligible due to the insulating sapphire substrate.[24] The initial 3–4 nm of the β-Ga_2O_3 film on sapphire may be insulating, because it is generally a mixed phase or polycrystalline consisting of both alpha Ga_2O_3 (α-Ga_2O_3) and β-Ga_2O_3 phases.[25,26] Hence, the total depth of the recess, depletion, and insulating layer is ~50 nm in the gated region in the recessed MOSFET, thus providing complete channel depletion, which result in E-mode transistor characteristics.[4] The schematic diagram of depletion depths resulting E-mode operation can be understood in Fig. 4(c).

The depletion depth analysis provides an approach to estimate the factors contributing to R_{on}. The total R_{on} of the recessed MOSFETs can be expressed as

$$R_{on} = 2R_C + R_D + R_S + R_{CH}, \quad (6)$$

where R_C is the metal-semiconductor contact resistance, R_D is the drain-gate resistance, R_S is the gate-source resistance, and R_{CH} is the channel resistance (under the gated region).

Here, the sheet resistance and contact resistance were calculated from the transfer length method (TLM) measurement. Using the depletion depth, device geometry, and sheet resistance (from TLM measurement), the calculated resistance values for the recessed MOSFETs were $2R_C = 59.5$ kΩ cm (15.2%), $R_D = 64.2$ kΩ cm (16.3%), $R_S = 64.2$ kΩ cm (16.3%), $R_{CH} = 205.1$ kΩ cm (52.2%), and $R_{Total} = 2R_C + R_D + R_S + R_{CH} = 393$ kΩ cm, which is nearer to R_{on} ~ 405 kΩ cm, calculated from the output curve of recessed MOSFETs. The major factor contributing to R_{on} in recessed MOSFETs is from the recess channel etching, which results in an increase in the sheet resistance, as similar as suggested by other reports.[27]

Since the non-recessed and recessed MOSFETs exhibit a D- and E-mode transistor behavior as shown in Figs. 3(a) and 3(c), an NMOS (DCFL) inverter can be fabricated by integrating D- and E-mode transistors as load and driver transistors, respectively. Figures 5(a) and 5(b) show a microscopic image and a circuit diagram of the depletion load NMOS inverter IC fabricated on the sapphire substrate, respectively. Figure 5(a) shows the voltage transfer characteristics (V_{TC}) for the NMOS inverter. The high-level output voltage (V_{OH}) is equal to the supply voltage (V_{DD}), confirming the D-load NMOS inverter operation. However, the low-level output voltage (V_{OL}) is greater than 0 V. Figure 5(b) shows the gain characteristics of the NMOS inverter at different V_{DD}. An inverter gain of ~2.5 was obtained at $V_{DD} = 9$ V, comparable with other recent GaN and Ga_2O_3-based inverters.[28,29]

To achieve a sharp inverter transition (high gain) and low (or zero) V_{OL}, a high load-to-driver resistance ratio α is required, as described as follows:

$$\alpha = \frac{R_L}{R_{DR}}, \quad (7)$$

where R_L and R_{DR} are the load and driver transistors' ON resistance, respectively.[30]

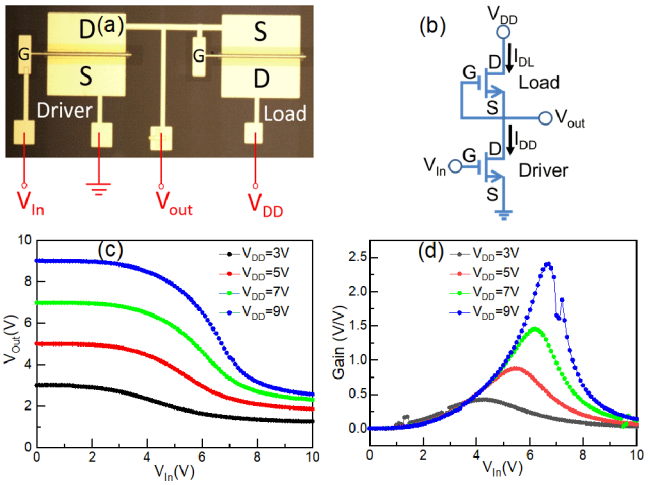

FIG. 5. Depletion load n-type metal oxide semiconductor (NMOS) inverter: (a) top microscopic view and (b) circuit diagram. Electrical characterization of the NMOS inverter: (c) voltage transfer curve and (d) voltage gain.

However, in our NMOS inverter, a poor α of ~0.5 was obtained, which is attributed to the high R_{on} of the E-mode MOSFET due to recess etching. α can be improved by increasing the channel width-to-length (W/L) ratio in the E-mode transistors, leading to an inverter with high voltage swing, sharp transition voltage, and a high noise margin.[30,31] Interdigited SD electrodes could enhance the W/L ratio of the transistor without further increase in the device size/area. Since R_{on} is directly proportional to the geometrical length of the device, a geometrically scaled E-mode MOSFET will exhibit low R_{on} and, hence, high α, which can also improve the NMOS inverter characteristics.

This study demonstrated heteroepitaxially grown E-mode β-Ga_2O_3 MOSFETs and NMOS inverter ICs on the low-cost sapphire substrate. The E-mode MOSFETs were enabled by using the gate recess technique. A MOSFET without a recessed gate exhibited D-mode characteristics. D- and E-mode MOSFETs showed a threshold voltage of −3.8 and 3 V with an on-off ratio of ~10^5, respectively. Furthermore, the monolithic integration of D- and E-mode transistors demonstrated Ga_2O_3 NMOS inverter IC operation with a gain of ~2.5 at $V_{DD} = 9$ V. The inverter performance could be improved by optimizing the W/L ratio and the geometrical scaling of the E-mode transistor to increase α. This work confirms the enormous potential of heteroepitaxial low-cost and scalable β-Ga_2O_3 MOSFETs and NMOS ICs for future integration with (ultra)wide bandgap devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts of interest to disclose.

Ethics Approval

This article does not contain any studies conducted by any of the authors that include humans or animals.

Author Contributions

Vishal Khandelwal: Conceptualization (equal); Data curation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **Saravanan Yuvaraja:** Conceptualization (equal); Writing – review & editing (equal). **Glen Issac Maciel Garcia:** Methodology (supporting); Writing – review & editing (supporting). **Chuanju Wang:** Data curation (supporting); Writing – review & editing (supporting). **Yi Lu:** Formal analysis (supporting); Writing – review & editing (equal). **Feras AlQatari:** Methodology (equal); Writing – review & editing (supporting). **Xiaohang Li:** Conceptualization (equal); Project administration (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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