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Demonstration of β-Ga_2O_3 nonvolatile flash memory for oxide electronics

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This report demonstrates an ultrawide bandgap β-Ga_2O_3 flash memory for the first time. The flash memory device realized on heteroepitaxial β-Ga_2O_3 film had TiN as the floating gate (FG) and Al_2O_3 as tunneling and gate oxides. A memory window of > 4 V was obtained between the programmed and erased states of the device. The memory states showed negligible degradation in threshold voltage (V_{TH}) even after 5000 s, exhibiting excellent nonvolatility. Furthermore, the device showed a V_{TH} of ~0.3 V after applying a 17 V programming voltage pulse, indicating the potential of the electron trapping phenomenon in the FG to achieve enhancement-mode operation in β-Ga_2O_3 transistors for high-power and logic applications. This study would provide insights for future oxide electronics integrating β-Ga_2O_3 memory.

(Ultra)wide bandgap oxides have tremendous application potential in transparent and flexible electronics, high power and RF electronics, UV photonics, and extreme environment electronics.[1–4)] To date, several oxide semiconductors such as indium gallium zinc oxide,[5)] In_2O_3,[6)] and β-Ga_2O_3[7)] have been widely explored in numerous applications including solid-state displays, thin-film transistors, power devices, and UV photodetectors. Among them, ultrawide bandgap β-Ga_2O_3 ($E_G \sim 4.9$ eV) has emerged as a promising candidate, especially for realizing oxide electronics, due to its superior properties including high-quality epitaxial films, wide n-type doping range from semi-insulating to highly conducting films, high chemical, and thermal stability.[7,8)] So far, β-Ga_2O_3-based power transistors,[9)] Schottky diodes,[10)] and solar-blind photodetectors[11)] have been extensively studied. However, β-Ga_2O_3-based memory devices are also required for realizing oxide electronics.

For memory devices, β-Ga_2O_3-based resistive random-access memory (RRAM) has been investigated.[12,13)] However, the filamentary behavior of β-Ga_2O_3 RRAMs and their precise control remains unclear. Moreover, β-Ga_2O_3 RRAMs will require integration with an appropriate selector device[14,15)] indicating a considerate effort is indispensable to achieve commercial maturity. Meanwhile, flash memory devices are a highly scalable alternative that exhibits substantial maturity due to decades of device exploration.[16,17)] Furthermore, trapping of electrons in the floating gate (FG) is a promising approach to realize enhancement-mode (E-mode) operation to get normally-OFF transistor operation.[18–20)] Thus, the development of β-Ga_2O_3-based flash memory devices is deemed to play a pivotal role in realizing future oxide electronics for various application fields.

In this work, we demonstrated a β-Ga_2O_3-based nonvolatile flash memory device using TiN metal as the FG. The virgin devices exhibited a normally-ON behavior, whereas positive and negative voltage pulses were applied for programming and erasing operation, respectively. A large memory of >4 V was obtained between the programming and erasing state with memory retention of > 5000 s. A large program bias is shown to shift the threshold voltage (V_{TH}), thereby promoting the E-mode operation. The β-Ga_2O_3 flash memory devices reported in this work showed a large nonvolatile memory window and a desirable memory retention characteristic.

Flash memory devices were fabricated on a 50 nm thick β-Ga_2O_3 film grown on a *c*-plane sapphire substrate. A pulsed laser deposition (PLD) system was employed to grow a heteroepitaxial film using a Si-doped β-Ga_2O_3 target. The growth temperature was maintained at 700 °C, whereas the laser ablation frequency and laser energy were set to 5 Hz and 100 mJ, respectively. The oxygen partial pressure was kept as 4 mTorr during growth. Post-growth, the samples were cleaned thoroughly using acid and acetone-IPA solvent treatment.

Next, flash memory devices with circular-geometry source/drain/gate contacts were fabricated. A cross-sectional schematic and top microscopic view of the fabricated devices are shown in Figs. 1(a) and 1(b). First, Ti/Au (20/100 nm) source/drain (SD) ohmic contacts were formed on the β-Ga_2O_3 film. Metals were deposited using a DC/RF sputtering system and patterned using the standard photolithography and lift-off process. The ohmic contacts were then annealed at 400 °C for 60 s in N_2 ambient. Thereafter, a 7 nm thick Al_2O_3 layer serving as the tunneling oxide was deposited using an atomic layer deposition (ALD) system at 250 °C. A 20 nm of TiN metal as the FG was then deposited on the tunneling oxide followed by the conventional photolithography and lift-off process for patterning. Next, a 25 nm thick Al_2O_3 blocking oxide was deposited using ALD at 250 °C. Finally, a TiN/Ti/Au (20/20/70 nm) control gate (CG) was formed using the sputtering and conventional photolithography process. TiN deposition was accomplished using a DC/RF sputtering system having a high-purity Ti target in the N_2 reactive chamber. Finally, the Al_2O_3 dielectric layer was removed to expose the SD ohmic contacts via BCl_3-based dry etching. The diameter of the drain contact was kept as 200 μm. A donut-shape CG had an inner circle and outer circle diameter of 220 and 280 μm, respectively,

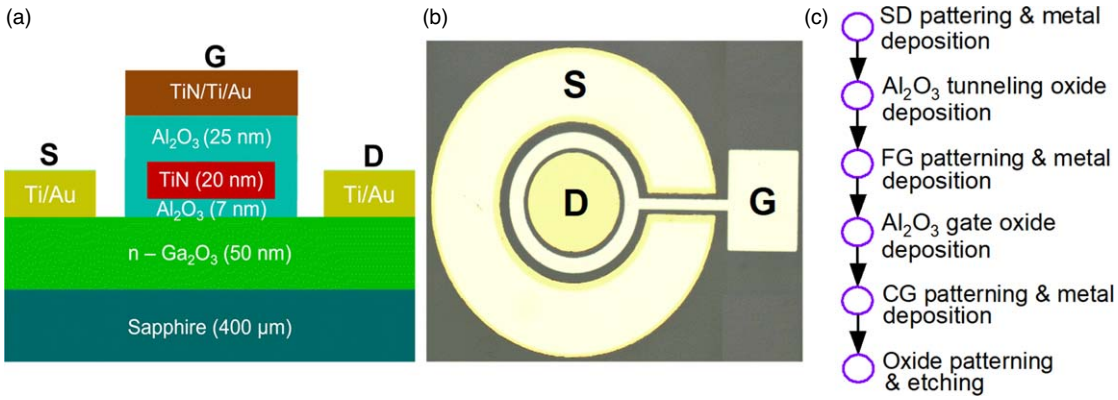

Fig. 1. β-Ga_2O_3 flash memory device (a) Cross-sectional schematic. (b) Top microscopic view. (c) Fabrication process flow.

indicating the effective (CG) gate length to be 30 μm. FG also had a donut-shape geometry (inner circle and outer circle diameter of 240 and 260 μm, respectively) and was kept within the boundaries of the CG. CG-to-drain and CG-to-source distances were kept as 10 μm and 20 μm, respectively. The device fabrication process flow is summarized in Fig. 1(c).

The epitaxial film quality was characterized using X-ray diffraction (XRD) and an atomic force microscope (AFM). The free carrier concentration inside the β-Ga_2O_3 film was measured using a Hall-effect measurement system. Electrical characterization was performed on a temperature-controlled probe station equipped with a Keithley 4200 semiconductor parameter analyzer setup.

The XRD pattern of the β-Ga_2O_3 film exhibited (−201), (−402), and (−603) peaks, as highlighted in Fig. 2(a) which confirms the mono-orientation of β-Ga_2O_3 film on the sapphire substrate. The RMS roughness of the film was observed to be ∼0.8 nm indicating a smooth surface morphology, as observed in the AFM image of Fig. 2(b). Based on the Hall-effect measurements, the electron concentration and mobility of the β-Ga_2O_3 film were found to be $\sim 5 \times 10^{18}$ cm^{-3} and 0.35 cm^{-2} V^{-1} s^{-1} at RT.

Next, the β-Ga_2O_3 flash memory devices were characterized to validate the nonvolatile memory operation. Figure 3(a) shows the transfer characteristics of the β-Ga_2O_3 flash memory device at $V_{DS} = 1$ V post application of program voltage pulses. The value of V_{TH} was estimated from the transfer characteristics using the extrapolation in the linear region method.[21] The virgin device showed a normally-ON behavior with a V_{TH} of −4.5 V. Subsequently, the application of different positive voltage pulses to the CG resulted in a positive V_{TH} shift, validating the programming operation of the memory, as shown in Fig. 3(a). For instance, a +17 V, 100 ms pulse applied to the CG yields a V_{TH} of ∼0.3 V. Note that such a positive value of V_{TH} in an n-channel transistor is identified as a normally-OFF device. For validating the erase operation, a virgin device was initially programmed to a V_{TH} of 0.3 V followed by the application of negative voltage pulses in the CG. Likewise, a negative V_{TH} shift was observed after the erase operation, as observed in Fig. 3(b). To validate the program/erase (P/E) repeatability, a virgin device was initially programmed followed by the erase operation. After the 1st program/erase (P/E) cycle, the device was tested for a 2nd P/E cycle, as highlighted in Fig. 3(c). Note that the virgin device and the device after 1st P/E cycle showed different sub-threshold slopes (SS). This can be attributed to the interface properties which are highly dependent on electron trapping/de-trapping phenomena, thereby influencing the SS after the 1st P/E cycle. Nevertheless, a reasonable P/E cycle repeatability after the 1st P/E cycle confirms the proof-of-concept working β-Ga_2O_3 flash memory device.

The dependence of the V_{TH} shift on the program/erase bias voltage is shown in Fig. 4(a). A nonvolatile memory window of greater than 4 V is achieved by applying program/erase pulses of less than 20 V in magnitude. Once programmed or erased, an insignificant V_{TH} shift was observed even after

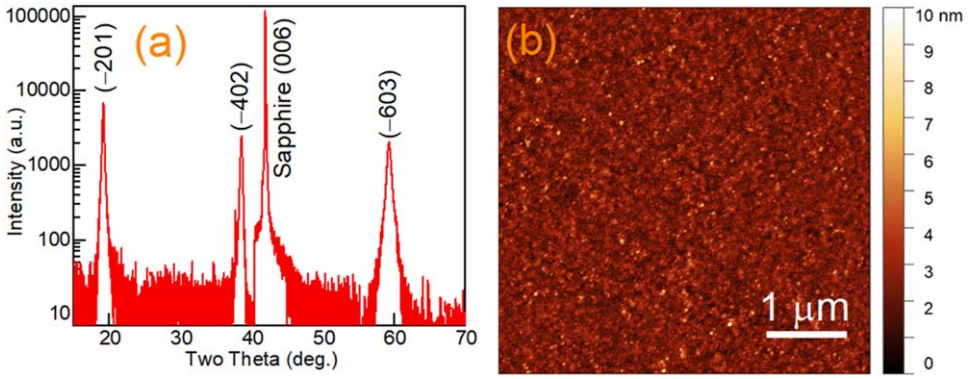

Fig. 2. Material quality of the β-Ga_2O_3 film on sapphire (a) XRD pattern highlighting the (−201), (−402), and (−603) peaks. (b) AFM surface morphology showing a smooth surface.

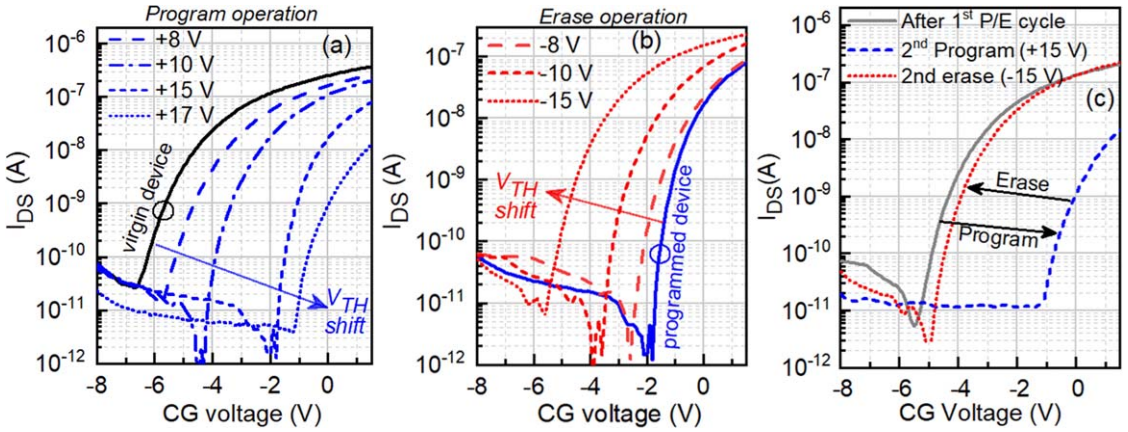

Fig. 3. Characteristics of β-Ga_2O_3 flash memory device at RT (a) Program characteristics, (b) Erase characteristics, (c) Program and erase characteristics after 1st P/E cycle.

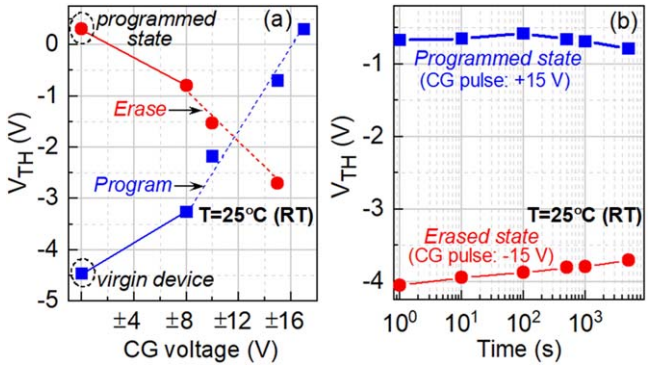

Fig. 4. Characteristics of β-Ga_2O_3 flash memory device at RT of $T = 25$ °C. (a) Measured V_{TH} of the device after the program and erase operations. (b) Retention characteristics.

5000 s, as shown in Fig. 4(b). Thus, the β-Ga_2O_3 flash memory showed excellent charge retention characteristics in its nonvolatile memory states.

Notably, the increase in V_{TH} during the program operation was observed to be higher than that during the erase operation [Fig. 4(a)]. For example, a CG pulse of +15 V during the program operation induced an effective V_{TH} shift (ΔV_{TH}) of ~4 V from the virgin state, whereas a CG bias of −15 V during the erase operation induced an effective ΔV_{TH} of ~3 V from the programmed state. We speculate that a lower V_{TH} shift in β-Ga_2O_3 flash memories during the erase operation was likely caused by the electric field distribution inside the films and carrier tunneling paths. The energy band profiles of the layers of the β-Ga_2O_3 flash memory layers in isolation (noncontact), during the program operation, and during the erase operation are shown in Figs. 5(a)–5(c), respectively. The work function and band energy details of TiN, β-Ga_2O_3, and Al_2O_3 can be found elsewhere.[22–24] During the program operation, the β-Ga_2O_3 channel is under accumulation. Since the Fermi energy level is close to the conduction band in n-type ultrawide bandgap semiconductors such as β-Ga_2O_3,[25] the program voltage pulse applied to the CG effectively caused a band-bending across the tunneling and blocking oxides, as highlighted in Fig. 5(b). However, the device V_{TH} was nearly positive at the programmed state. Thus, a relatively larger area of β-Ga_2O_3 film under the gate is fully depleted when electrons are stored in the FG after the program operation. Therefore, a portion of the erase voltage pulse applied to the CG was sustained by the depleted β-Ga_2O_3 film along with the tunneling and blocking oxides, as highlighted in Fig. 5(c). Moreover, to obtain a similar V_{TH} shift, the desired erase pulse duration was observed to be significantly higher than the program pulse duration (not shown). All of these observations exhibited good agreement with the conventional FG or charge-trap NAND flash memories realized on Si.[17,26] Note that the device $|V_{TH}|$ after the erase operation was observed to be lower than $|V_{TH}|$ of the virgin device indicating the erase operation was unable to remove all the electrons injected into the FG during the program operation. Moreover, improving the erase characteristics by hole injection into the FG is an unlikely case for β-Ga_2O_3 flash memories. Traditionally, planar Si flash memories are fabricated on a p-type substrate,[27] whereas 3D-NAND flash memories are fabricated on poly-Si

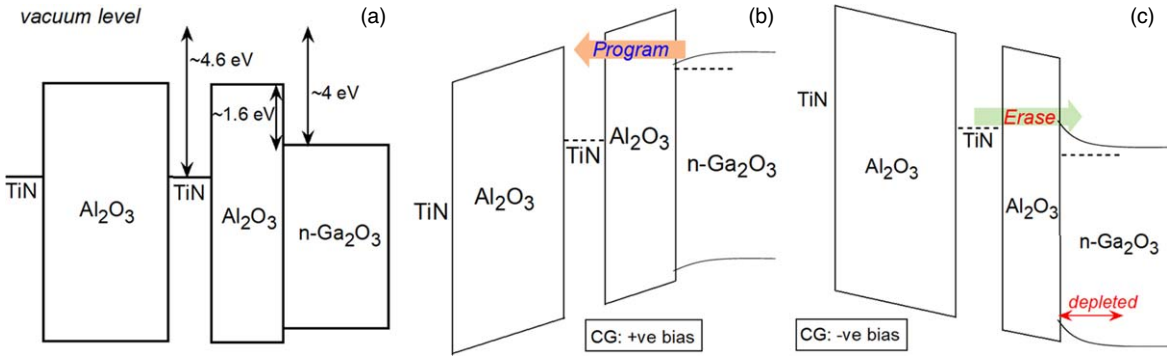

Fig. 5. Schematics of energy band profile along vertical outline through the CG (a) Isolated (noncontact) layers. During (b) program operation (c) erase operation.

pillars.[28)] During the erase operation, holes can be injected from the channel to the charge-trap layer which is between the tunneling oxide and gate oxide layers.[29,30)] Therefore, the choice of proper hole charge-trap dielectric has been observed to improve the erase characteristics of both planar and 3D Si flash memories.[27,28)] In contrast, a low intrinsic carrier concentration in β-Ga_2O_3 indicates the channel is free from holes during the erase operation. Moreover, obtaining a p-type β-Ga_2O_3 is also a major challenge.[8)] Thus, program and erase operation in β-Ga_2O_3 flash memories are thought to be solely due to electron injection and removal from the FG.

We now discuss the contributions of this work apart from data storage via β-Ga_2O_3 memory. As observed in Fig. 4(a), a program bias voltage pulse of $\geqslant$ 17 V results in a normally-OFF transistor ($V_{TH} > 0$ V). Therefore, a programmed β-Ga_2O_3 flash memory device can be used to realize standalone normally-OFF low-voltage transistors. Moreover, both high-voltage and low-voltage power switches are controlled by logic circuitry such as pulse width modulators. Traditionally, Si-based CMOS technology is used to realize this logic control circuitry. However, β-Ga_2O_3 based all-oxide electronics mandates these circuits to be realized on a native substrate. Unfortunately, the non-availability of appropriate p-type doping in β-Ga_2O_3 poses a major hindrance in realizing CMOS logic operations. Interestingly, many of these logic control circuitries can be realized using a combination of normally-ON and normally-OFF transistors.[31)] Thus, the logic circuitry for controlling the β-Ga_2O_3 power converters can be realized using a suitable connection of virgin/erased (normally-ON) β-Ga_2O_3 flash memory device with a programmed (normally-OFF) β-Ga_2O_3 flash memory device. Consequently, the power converters and their logic control circuitry can be monolithically integrated into a standalone β-Ga_2O_3 substrate. Finally, the flash memories reported in this work were fabricated on a foreign substrate indicating the compatibility of the β-Ga_2O_3 flash memory devices with low-cost heterogeneous integration schemes. Note that the devices investigated in this work were free from the post-deposition annealing (PDA) step. However, PDA has been observed to minimize the trap density at the Al_2O_3/β-Ga_2O_3 interface thereby improving the overall interface quality.[32,33)] Therefore, a realistic β-Ga_2O_3 flash memory processing may require a PDA step to obtain a good tunnel oxide interface—which is critical for memory operations.

In summary, we demonstrated β-Ga_2O_3 flash memory transistors using a TiN metal FG. A large nonvolatile memory window of $>$ 4 V was observed between the programmed and erased states. The memory exhibited an insignificant threshold voltage shift in the programmed and erased states even after 5000 s. Finally, the realization of enhancement-mode operation by storing electrons in the FG is thought to be promising for realizing multiple essential devices of β-Ga_2O_3 electronics.

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